UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,506	04/12/2001	Sung Soo Chung	CISCO-3024	5788

49715   7590   10/05/2005

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EXAMINER
CHAUDRY, MUJTABA M

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/834,506	CHUNG ET AL.
	Examiner	Art Unit
	Mujtaba K. Chaudry	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 September 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13,25 and 26* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

A terminal disclaimer was received on September 08, 2005, which overcomes the double

patenting rejection.

Response to Amendment

Upon further reconsideration, Applicants' arguments/amendments with respect to pending claims

1-8, 13, 25 and 26 filed March 18, 2005 have been fully reconsidered but are not persuasive for

the following reasons.

      Applicants contend, "...the claims include the term AC coupled interconnection while the

prior art of Gruetzner uses the term AC interconnection...the two are no synonymous..." The

Examiner respectfully disagrees. An AC interconnection has to be coupled for it to be

interconnected. Applicants further point to the specification of the present application to

elaborate on the definition of AC coupled interconnection. The Examiner would like to point out

a teaching reference (not used in the rejection), Whetsel teaches in Figures 1 and 2 a DC and AC

interconnect that are connected by a capacitor. Although the prior art of record, Gruetzner, does

not explicitly state the word capacitor as pointed out by the Applicants, it is well understood in

the art, as shown by Whetsel, that AC interconnects are capacitively coupled.

The Examiner disagrees with the Applicant and maintains rejections with respect to pending claims 1-8, 13, 25 and 26. All arguments have been considered. It is the Examiner's conclusion that pending claims 1-8, 13, 25 and 26 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8,13, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims recite, "...the run-test/idle state..." which is not clear if it is *a run-test state and a idle state* or *a run-test state or a idle state*. However, it is not clear how the test controller could be in both states at the same time?

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.

    4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8, 13, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gruetzner et al. (USPN 5444715) further in view of Parker et al. (USPN 5513188).

    As per claims 1, 5, 13, 25 and 26, Gruetzner et al. (herein after: Gruetzner) substantially

teaches (title, abstract and Figure 1) to test AC interconnects of integrated circuits. An integrated

circuit chip (110) adapted to provide interconnect capability and an AC interconnect test method

therefor. Test and control data are scanned in the scan-path of latches (114 and 115) to initialize

the AC interconnect test. Subsequently, applying the functional system clocks via lines 118 and

128 simulates the functional system mode. Particularly, Gruetzner teaches (Figure 1) a driving

circuit (110) and a receiving circuit (111). The sending chip 110 comprises a driver 122 which is

interconnected to a master slave latch 114 via line 120. Further the driver 122 is interconnected

with a master slave latch 115 via the line 121. The slave latch S of the master slave latch 114

and the master latch M of the master slave latch 115 are interconnected via line 119. The slave

latches S of the master slave latches 114 and 115 are clocked by the slave clock via line 118.

The interconnected master slave latches 114 and 115 constitute a scan-path, whereby data are

scanned-in via line 112 and scanned-out via line 113. In functional system mode data are input

into the master slave latches 114 and 115 via lines 116 and 117 respectively. The receiving chip

111 comprises a receiver 123 as well as a master slave latch 125. The master slave latch 125

constitutes or forms part of a scan-path, whereby data are scanned-in the scan-path via line 126

and scanned-out via line 127. The master latch M of the master slave latch 125 is clocked by the

master clock via line 128. In normal functional system mode data is input into the master slave

latch 125 by the receiver 123, whereas data is output from the slave S of the master slave latch

125 via line 129 to subsequent circuit elements. The driver 122 and the receiver 123 of the two

chips are interconnected by line 124 which in this case is a bus. If the AC interconnect test is to

be performed, first the test data which is to be transmitted by the driver 122 is stored in the

master M of the master slave flip-flop 114. In the preferred embodiment, the driver 122 is

implemented as a three state driver. A logical zero input via line 121 into the driver disables the

driver, whereas a logical one enables the driver. Thus the corresponding control data is stored in

the master M of the master slave latch 115. Further it is advantageous to store the inverted test

data which is stored in the master of the master slave flip-flop 114 in the master slave flip-flop

125 of the receiving chip 111. Second, after this initialization is performed, the normal functional

system mode is simulated by applying the normal slave clock via line 118 as indicated by the

timing diagram of FIG. 2 by the signal "SLAVE CLOCK". Thereby the data stored in both of

the master latches M of the master slave latches 114 and 115 is input into the driver 122 via the

lines 120 and 121, respectively. This is indicated by the signals "DATA-IN" and "DRIVER HZ

CNTL", respectively, shown in the timing diagram of FIG. 2. After a certain time delay the

receiver 123 receives the test data as it is indicated by the signal "receiver-in" of the timing

diagram in FIG. 2. The data received by the receiver 123 in the receiving chip 111 is latched in

the master M of the master slave flip-flop 125 by the following master clock signal which is

transmitted via line 128. This is also shown by the signal "MASTER CLOCK" shown in FIG. 2.

Subsequently the received data is scanned-out via line 127 and compared to the expected result.

Gruetzner does not explicitly teach the driving circuit and the receiving circuit to have a

plurality of boundary scan cells as indicated in the present application.

However, Parker et al. (herein after: Parker) teaches (title and abstract) a method for

generating improved detection and diagnostic test patterns and for improving the diagnostic

resolution of interconnect testing of a circuit. In a first embodiment, an optimal boundary-scan

test pattern is generated. In a second embodiment, boundary-scan test diagnosis is enhanced by

utilizing x,y coordinate data corresponding to the physical location of devices on the tested

circuit. In a third embodiment, diagnosis of unpowered short-circuit testing is enhanced.

Particularly, Parker teaches (Figure 2 and cols. 2-3) a test access port (TAP) controller 118 is a

state machine which controls boundary register 102. Five I/O terminals have been added to

chip 100 to accommodate boundary-scan. These five terminals constitute the test access

port (TAP). A TDI (test data in) terminal provides serial test data and instruction bits to

scanpath 110. A TDO (test data out) terminal provides serial output for scanpath 110. A TCK

(test clock) terminal provides an independent test clock to chip 100. A TMS (test mode select)

terminal provides the logic levels needed to change the state of TAP controller 118. A TRST

(test rest) terminal is used to reset chip 100. Circuit 200 includes six interconnected IC's U1-U6.

Boundary register cells 104 are shown in each IC. A scanpath 110 is shown connecting register

cells 104 of IC's U1-U6. Cells 104 in scanpath 110 form the boundary register (102 in FIG. 1).

The method of boundary-scan interconnect testing circuit 200 is shown in FIG. 3. At step 302,

a test vector (i.e., test data) is serially shifted into boundary register 102. At step 304, the test

vector is broadcast from appropriate output buffers (drivers) over the corresponding nets to

receiving input buffers. The broadcast data is then captured into the receiving register cells at

step 306. The captured test data is shifted out of boundary register 102 at step 308. Finally, the

captured test data is compared to the broadcast test data at step 310. Differences in the captured

and broadcast data indicate a fault. Because the captured test data contains information on the

condition of the net over which it was broadcast, it is also called a "net signature" herein.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention

was made to incorporate the boundary scan testing technique with the testing apparatus of

Gruetzner. This modification would have been obvious to one of ordinary skill because one of

ordinary skill would have recognized that utilizing boundary scan testing would have enhanced

diagnostic resolution of circuit interconnects.

As per claims 2, 4, 6 and 8, Gruetzner substantially teaches, in view of above rejections,

(col. 3) the test data which are received in the receiving chip are subsequently shifted out to

compare the received data with the sent data. Gruetzner teaches to initialize the scan-path of the

receiving chip with the inverted test data which are scanned-in the scan-path of the sending

chip. This is to monitor data transitions in the scan-path of the receiving chip due to data

received from the sending chip.

As per claims 3 and 7, Gruetzner substantially teaches, in view of above rejections, (col.

3) random test data are scanned-in the scan-path of the sending chip and the AC interconnect test

is repeated several times, scanning-in the inverted test data into the scan-path of the receiving

chip is not necessary. This is due to the low probability that an accidental match of the initial

data stored in the scan-path of the receiving chip and the test data, which is to be transmitted by

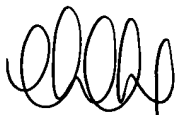the sending chip, occurs several times in sequence.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.
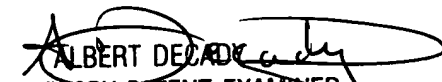
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
September 27, 2005

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